AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

1-21. (Canceled)

22. (Currently Amended) An MOS transistor formed on a semiconductor substrate of a first conductivity type comprising:

(a) an interfacial layer formed on the substrate;

(b) a high dielectric constant layer formed on the interfacial layer that comprises a material that is selected from the group consisting of Ta_2O_5, $Ta_2(O_{1-x}N_x)_5$ wherein x ranges from greater than 0 to 0.6, a solid solution of $(Ta_2O_5)_r$-$(TiO_2)_{1-r}$ wherein r ranges from about 0.9 to less than 1, a solid solution $(Ta_2O_5)_s$-$(Al_2O_3)_{1-s}$ wherein s ranges from 0.9 to less than 1, a solid solution of $(Ta_2O_5)_t$-$(ZrO_2)_{1-t}$ wherein t ranges from about 0.9 to less than 1, a solid solution of $(Ta_2O_5)_u$-$(HfO_2)_{1-u}$ wherein u ranges from about 0.9 to less than 1, and mixtures thereof wherein the interfacial layer separates the high dielectric constant layer from the substrate;

(c) a gate electrode having a width of less than 0.3 micron covering the high dielectric constant layer;

(d) first and second lightly doped regions of a second conductivity type disposed on respective areas of the substrate surface;

(e) a source and drain regions of a second conductivity type; [[and]]

(f) a pair of first non-conductive spacers formed adjacent to the gate electrode and formed on the high dielectric constant layer; and

(g) a pair of second non-conductive spacers that are adjacent to the first spacers and the high dielectric constant layer.

23. (Original) The MOS transistor of claim 22 comprising:

(g) an insulator layer covering the device and defining a first contact hole that is filled with a first contact material and a second contact hole that are filled with a second contact material, wherein the insulator layer has a substantially planar surface.

24. (Currently Amended) The MOS transistor of claim 22 wherein the gate electrode is formed from a metal that is selected from the group consisting of TiN, W, Ta, [[MO]] Mo and multilayers thereof.

25. (Original) The MOS transistor claim 22 wherein the gate electrode comprises doped polysilicon.

26. (Original) The MOS transistor of claim 25 comprising a barrier layer between the gate electrode and the high dielectric constant layer.

27. (Currently Amended) The MOS transistor of claim 22 ~~comprising a~~ wherein the pair of second spacers that are adjacent to the first spacers [[and]] are formed [[on]] over the lightly doped regions.

28. (Original) The MOS transistor of claim 22 comprising a silicide layer on the source and drain regions.

29. (Original) The MOS transistor of claim 22 wherein the high dielectric constant material layer has a thickness that ranges from about 4 nm to 12 nm.

30. (Original) The MOS transistor of claim 22 wherein the high dielectric constant material is Ta_2O_5.

31. (Previously Presented) The MOS transistor of claim 22 wherein the high dielectric constant material is $Ta_2(O_{1-x}N_x)_5$ wherein x ranges from greater than 0 to 0.6.

32. (Previously Presented) The MOS transistor of claim 22 herein the high dielectric constant material is a solid solution of $(Ta_2O_5)_r$-$(TiO_2)_{1-r}$ wherein r ranges from about 0.9 to less than 1.

33. (Previously Presented) The MOS transistor of claim 22 wherein the high dielectric constant material is a solid solution $(Ta_2O_5)_s$-$(Al_2O_3)_{1-s}$ wherein s ranges from 0.9 to less than 1.

34. (Previously Presented) The MOS transistor of claim 22 wherein the high dielectric constant material is a solid solution $(Ta_2O_5)_t$-$(ZrO_2)_{1-t}$ wherein t ranges from about 0.9 to less than 1.

35. (Previously Presented) The MOS transistor of claim 22 wherein the high dielectric constant material is a solid solution of $(Ta_2O_5)_u$-$(HfO_2)_{1-u}$ wherein u ranges from about 0.9 to less than 1.

36. (Original) The MOS transistor of claim 22 wherein the substrate comprises silicon.

37. (Original) The MOS transistor of claim 22 wherein the first spacers comprise an oxide or nitride material.

38. (Currently Amended) An MOS transistor formed on a semiconductor substrate of a first conductivity type comprising:

(a) an interfacial layer formed on the substrate, wherein the interfacial layer comprises silicon nitride;

(b) a high dielectric constant layer formed on the interfacial layer that comprises a material that is selected from the group consisting of Ta_2O_5, $Ta_2(O_{1-x}N_x)_5$ wherein x ranges from greater than 0 to 0.6, a solid solution of $(Ta_2O_5)_r$-$(TiO_2)_{1-r}$ wherein r ranges from about 0.9 to less than 1, a solid solution $(Ta_2O_5)_s$-$(Al_2O_3)_{1-s}$ wherein s ranges from 0.9 to less than 1, a solid solution of $(Ta_2O_5)_t$-$(ZrO_2)_{1-t}$ wherein t ranges from about 0.9 to less than 1, a solid solution of $(Ta_2O_5)_u$-$(HfO_2)_{1-u}$ wherein u ranges from about 0.9 to less than 1, and mixtures thereof wherein the interfacial layer separates the high dielectric constant layer from the substrate;

(c) a gate electrode having a width of less than 0.3 micron covering the high dielectric constant layer;

(d) first and second lightly doped regions of a second conductivity type disposed on respective areas of the substrate surface;

(e) a source and drain regions of a second conductivity type; [[and]]

(f) a pair of first non-conductive spacers formed adjacent to the gate electrode and formed on the high dielectric constant layer; and

(g) a pair of second non-conductive spacers that are adjacent to the first spacers and the high dielectric constant layer.

39. (Currently Amended) An MOS transistor formed on a semiconductor substrate of a first conductivity type comprising:

(a) an interfacial layer formed on the substrate, wherein the interfacial layer comprises silicon oxynitride;

(b) a high dielectric constant layer formed on the interfacial layer that comprises a material that is selected from the group consisting of Ta_2O_5, $Ta_2(O_{1-x}N_x)_5$ wherein x ranges from greater than 0 to 0.6, a solid solution of $(Ta_2O_5)_r$-$(TiO_2)_{1-r}$ wherein r ranges from about 0.9 to less than 1, a solid solution $(Ta_2O_5)_s$-$(Al_2O_3)_{1-s}$ wherein s ranges from 0.9 to less than 1, a solid solution of $(Ta_2O_5)_t$-$(ZrO_2)_{1-t}$ wherein t ranges from about 0.9 to less than 1, a solid solution of $(Ta_2O_5)_u$-$(HfO_2)_{1-u}$ wherein u ranges from about 0.9 to less than 1, and mixtures thereof wherein the interfacial layer separates the high dielectric constant layer from the substrate;

(c) a gate electrode having a width of less than 0.3 micron covering the high dielectric constant layer;

(d) first and second lightly doped regions of a second conductivity type disposed on respective areas of the substrate surface;

(e) a source and drain regions of a second conductivity type; [[and]]

(f) a pair of first non-conductive spacers formed adjacent to the gate electrode and formed on the high dielectric constant layer; and

(g) a pair of second non-conductive spacers that are adjacent to the first spacers and the high dielectric constant layer.

40. (Previously Presented) The MOS transistor of Claim 22, wherein the interfacial layer comprises silicon oxide.

41. (New) The MOS transistor of Claim 22, wherein the pair of second non-conductive spacers are formed on the interfacial layer.

42. (New) The MOS transistor of Claim 38, wherein the pair of second non-conductive spacers are formed on the interfacial layer.

43. (New) The MOS transistor of Claim 39, wherein the pair of second non-conductive spacers are formed on the interfacial layer.